PHD THESIS SUBJECT PROPOSAL #27-7

Title: Design and Optimization of a Low-Power Digital CMOS Neural Accelerator for Edge AI

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Proposal Summary:

The rapid development of artificial intelligence (AI), particularly deep learning and artificial neural networks, has led to an increasing demand for high-performance computing architectures capable of executing complex inference tasks under strict energy, area, and latency constraints. Although graphics processing units provide significant computational capabilities, their power consumption, implementation complexity, memory requirements, and overall cost may limit their deployment in resource-constrained edge devices. This doctoral research aims to design, optimize, and validate a specialized low-power digital CMOS neural accelerator dedicated to the execution of lightweight artificial neural networks for Edge AI applications. The proposed architecture will be developed through a hardware–algorithm co-design methodology that considers the computational characteristics of neural networks alongside the constraints of digital integrated circuit implementation.